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(54) **ORGANIC LIGHT EMITTING DIODE  
DISPLAY PANEL AND MANUFACTURING  
METHOD THEREOF**

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(57) **ABSTRACT**

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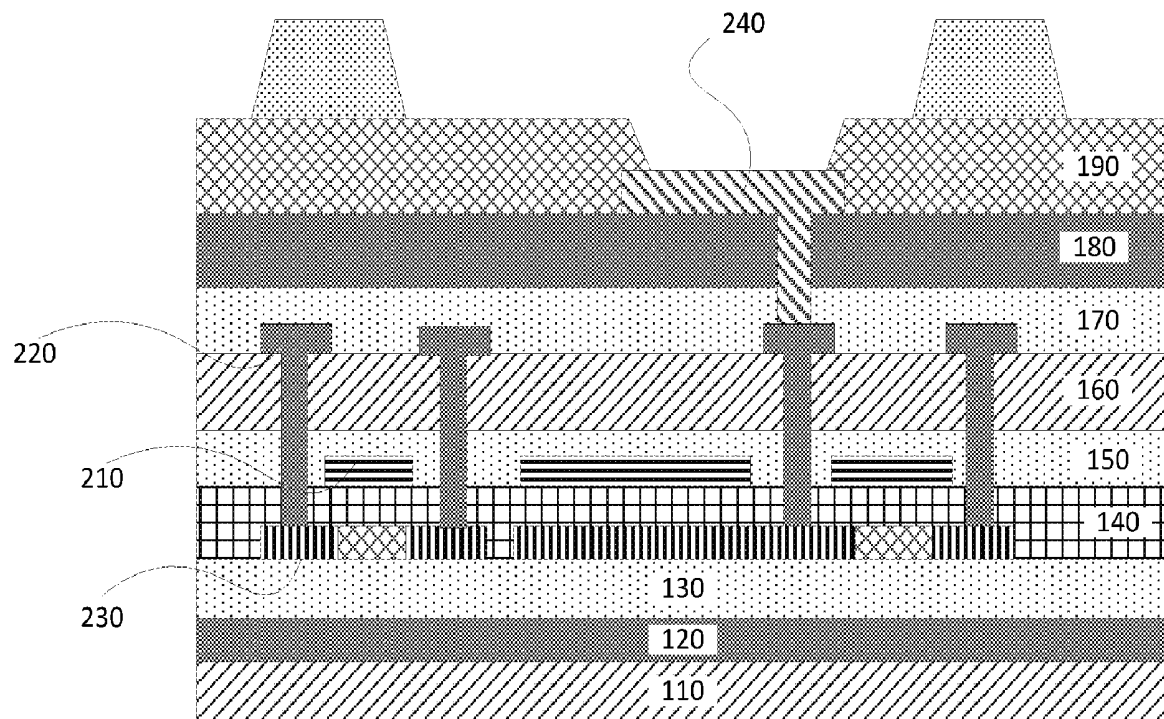
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Oct. 18, 2018 (CN) ..... 201811213431.0

An organic light emitting diode (OLED) display panel and manufacturing method thereof are provided. The display panel includes a substrate, a thin film transistor layer, and a light emitting structure, wherein the thin film transistor layer includes a polysilicon layer, a gate dielectric layer positioned on the polysilicon layer, a gate metal layer positioned on the gate dielectric layer, a gate buffer layer positioned on the gate dielectric layer, and an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer.



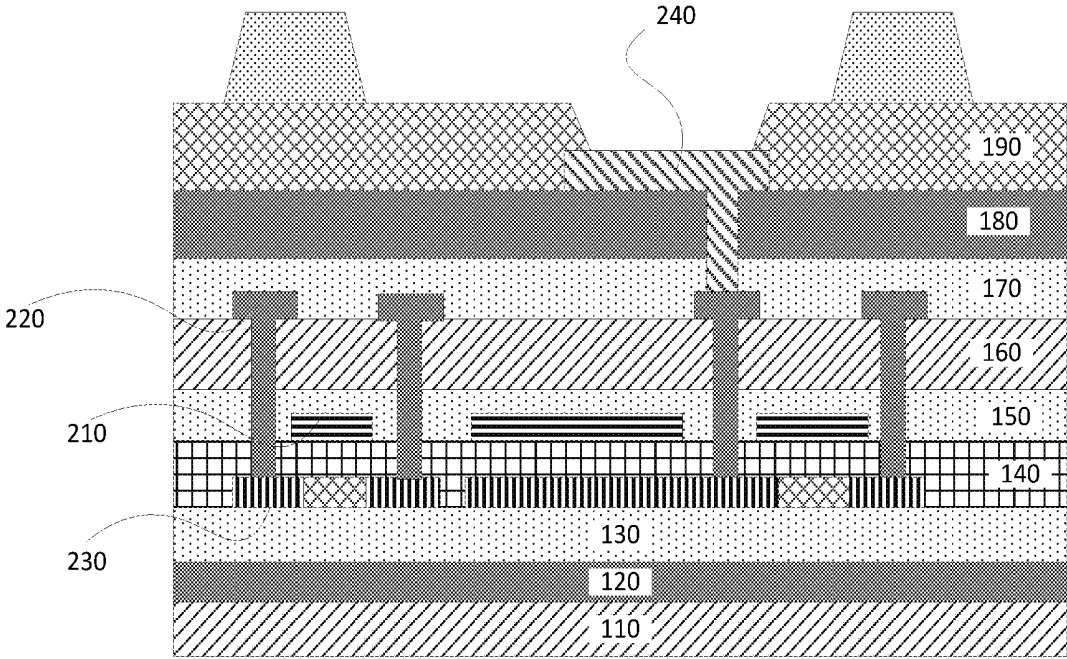


FIG. 1

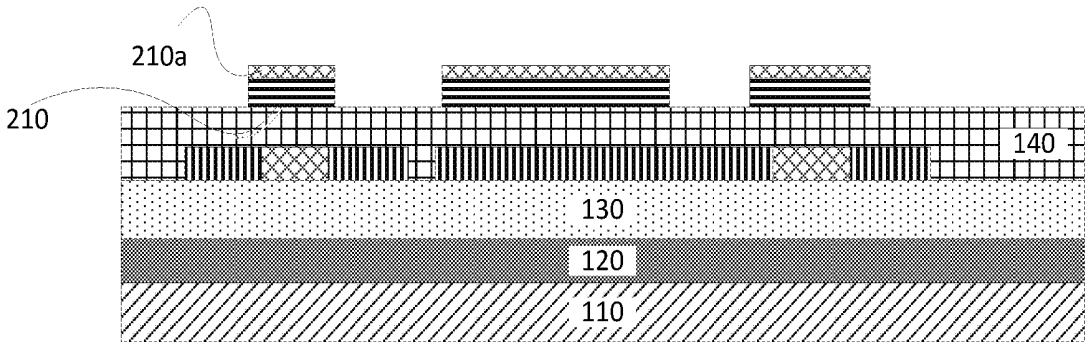


FIG. 2

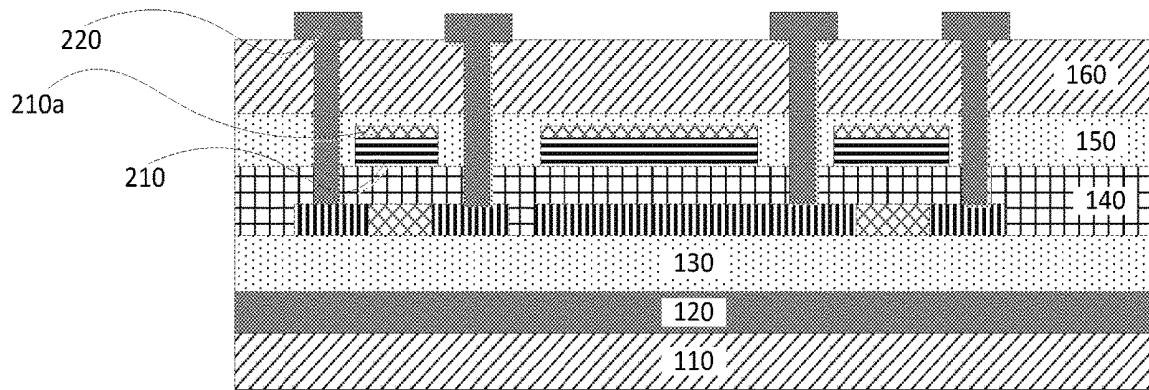


FIG. 3

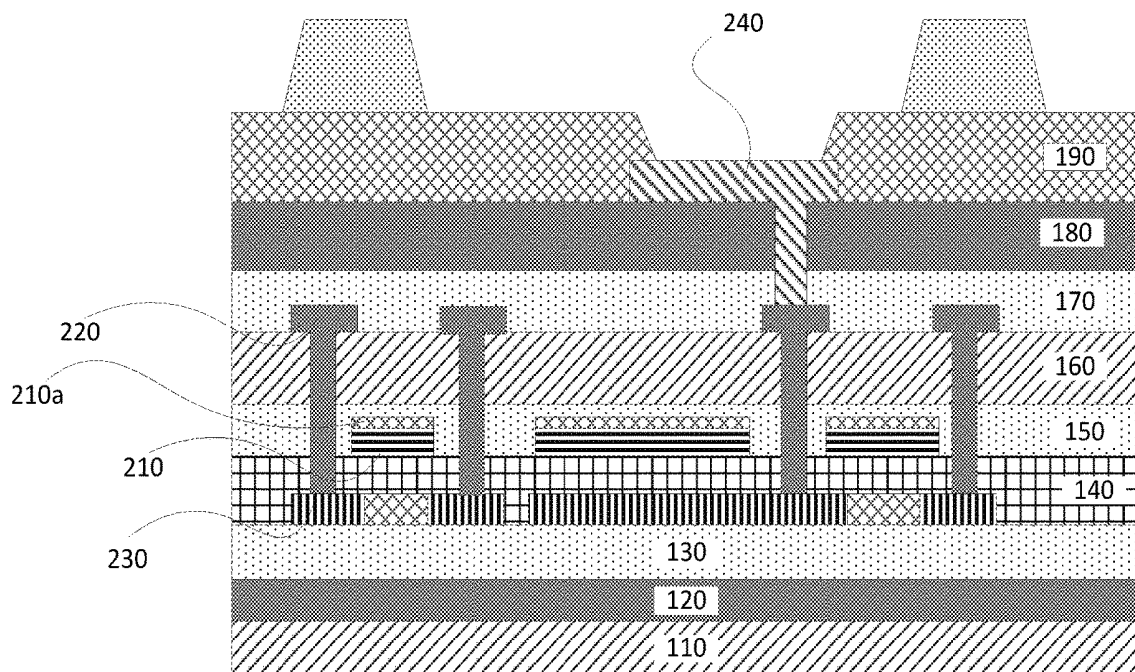


FIG. 4

**ORGANIC LIGHT EMITTING DIODE  
DISPLAY PANEL AND MANUFACTURING  
METHOD THEREOF**

CROSS REFERENCE TO RELATED  
APPLICATION

[0001] This application claims the priority of International Application No. PCT/CN2018/116985, filed on 2018 Nov. 22, which claims priority to Chinese Application No. 201811213431.0, filed on 2018 Oct. 18. The entire disclosures of each of the above applications are incorporated herein by reference.

BACKGROUND OF INVENTION

Field of Invention

[0002] The present invention relates to the field of display technologies, and in particular, to an organic light emitting diode display panel and manufacturing method thereof.

Description of Prior Art

[0003] In the manufacture process of the thin film transistor in a conventional organic light emitting diode (OLED) display panel, an interlayer dielectric layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) after the gate metal is completed. At present, the gate metal is usually made of molybdenum (Mo), and the interlayer dielectric layer is usually made of a laminate of silicon oxide (SiO<sub>x</sub>) and silicon nitride (SiN<sub>x</sub>).

Technical Problems

[0004] Since there is a large degree of difference regarding material properties of molybdenum and silicon oxide, there is often a large stress at their interface, whereby molybdenum and silicon oxide cannot be tightly bonded. The stress between them even causes the interlayer dielectric layer to fall off, and generate a gap between the gate metal and the interlayer dielectric layer, thereby seriously affecting the characteristics of the thin film transistor, and seriously affecting the yield of the device.

SUMMARY OF THE INVENTION

Technical Solutions

[0005] The present invention provides an organic light emitting diode display panel and manufacturing method thereof, which could solve the technical problem of the film layer falling off due to the stress between the interlayer dielectric layer and the gate metal in the prior art.

[0006] In order to solve the above problems, the present invention provides an organic light emitting diode (OLED) display panel, wherein the display panel includes a substrate, a thin film transistor layer positioned on the substrate, and a light emitting structure positioned on the thin film transistor layer and connected to a source/drain region trace layer in the thin film transistor layer;

[0007] wherein the thin film transistor layer includes:

[0008] a polysilicon layer positioned on the substrate, the polysilicon layer has heavily doped source/drain regions spaced from each other a distance and a lightly doped channel region located between the source/ drain regions;

[0009] a gate dielectric layer positioned on the polysilicon layer;

[0010] a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

[0011] a gate buffer layer positioned on the gate dielectric layer; and

[0012] an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

[0013] wherein the source/drain region trace layer penetrates through the gate dielectric layer and the interlayer dielectric layer; and

[0014] wherein a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

[0015] According to one aspect of the invention, a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

[0016] According to one aspect of the invention, the interlayer dielectric layer includes a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

[0017] In order to solve the above problems, the present invention provides an organic light emitting diode (OLED) display panel, wherein the display panel includes a substrate, a thin film transistor layer positioned on the substrate, and a light emitting structure positioned on the thin film transistor layer and connected to a source/drain region trace layer in the thin film transistor layer;

[0018] wherein the thin film transistor layer includes:

[0019] a polysilicon layer positioned on the substrate, the polysilicon layer has heavily doped source/drain regions spaced from each other a distance and a lightly doped channel region located between the source/drain regions;

[0020] a gate dielectric layer positioned on the polysilicon layer;

[0021] a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

[0022] a gate buffer layer positioned on the gate dielectric layer; and

[0023] an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

[0024] wherein the source/drain region trace layer penetrates through the gate dielectric layer and the interlayer dielectric layer.

[0025] According to one aspect of the invention, a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

[0026] According to one aspect of the invention, a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

[0027] According to one aspect of the invention, the interlayer dielectric layer includes a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is

positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

[0028] According to one aspect of the invention, the gate buffer layer has a thickness of 2 to 5 nm.

[0029] In order to solve the above problems, the present invention provides a method of manufacturing an organic light emitting diode (OLED) display panel, wherein the method includes the steps of:

[0030] providing a substrate;

[0031] forming a polysilicon layer positioned on the substrate, forming heavily doped source/drain regions in the polysilicon layer, the source/drain regions being spaced from each other a distance, and a lightly doped channel region in the polysilicon layer and between the source/drain regions;

[0032] forming a gate dielectric layer positioned on the polysilicon layer;

[0033] forming a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

[0034] forming a gate buffer layer positioned on the gate dielectric layer;

[0035] forming an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

[0036] forming a source/drain region trace layer penetrating through the gate dielectric layer and the interlayer dielectric layer; and

[0037] forming a light emitting structure connected to the source/drain region trace layer.

[0038] According to one aspect of the invention, a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

[0039] According to one aspect of the invention, a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

[0040] According to one aspect of the invention, the interlayer dielectric layer includes a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

[0041] According to one aspect of the invention, the gate buffer layer has a thickness of 2 to 5 nm.

#### Advantageous Effects

[0042] The present invention improves the existing thin film transistor of the organic light emitting diode display panel and the manufacturing method thereof. After the gate metal (molybdenum) is completed, a thin layer of dense molybdenum oxide of about 2 to 5 nm is formed as a gate buffer layer over the gate dielectric layer by oxidation, and then an interlayer dielectric layer is deposited. Since the surface tension of the molybdenum oxide is between the surface tension of the molybdenum and the surface tension of the interlayer dielectric layer, the molybdenum oxide can effectively reduce the interface stress between the gate metal and the interlayer dielectric layer to prevent the occurrence of falling off after deposition of the interlayer dielectric layer, whereby the characteristics of the thin film transistor can be improved, and the yield of the device can be greatly increased.

#### BRIEF DESCRIPTION OF DRAWINGS

[0043] In order to describe clearly the embodiment in the present disclosure or the prior art, the following will introduce the drawings for the embodiment shortly. Obviously, the following description is only a few embodiments, for the common technical personnel in the field it is easy to acquire some other drawings without creative work.

[0044] FIG. 1 is a structure diagram of a thin film transistor in an organic light emitting diode display panel in the prior art; and

[0045] FIG. 2 to FIG. 4 are structure diagrams showing the structure of a thin film transistor in each step of a method for manufacturing an organic light emitting diode display panel according to an embodiment of the present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0046] The description of following embodiment, with reference to the accompanying drawings, is used to exemplify specific embodiments which may be carried out in the present disclosure. Directional terms mentioned in the present disclosure, such as “top”, “bottom”, “front”, “back”, “left”, “right”, “inside”, “outside”, “side”, etc., are only used with reference to the orientation of the accompanying drawings. Therefore, the used directional terms are intended to illustrate, but not to limit, the present disclosure. In the drawings, the components having similar structures are denoted by same numerals.

[0047] First, the prior art is briefly described. Referring to FIG. 1, a thin film transistor layer of an organic light emitting diode display panel of prior art includes a substrate 110, a silicon nitride layer 120, a silicon oxide layer 130, a polysilicon layer 140, a gate metal 210, and a first interlayer dielectric layer 150, a second interlayer dielectric layer 160, source/drain metal traces 220, a first insulating layer 170, a second insulating layer 180, an anode metal 240, and a pixel defining layer 190.

[0048] The substrate 110 is usually a rigid substrate such as glass, or a flexible substrate such as a polyimide substrate.

[0049] The silicon nitride layer 120 is located on the substrate 110, and the silicon oxide layer 130 is located on the silicon nitride layer 120.

[0050] The polysilicon layer 140 is located on the silicon oxide layer 130, and the polysilicon layer 140 includes a heavily doped source and drain regions 230 and a channel region between the source and drain regions 230.

[0051] The gate metal 210 is located on the polysilicon layer 140, and the gate metal 210 covers the polysilicon layer 140 above the channel region.

[0052] The first interlayer dielectric layer 150 is located on the polysilicon layer 140, and the first interlayer dielectric layer 150 covers the gate metal 210 and the polysilicon layer 140 not covered by the gate metal 210.

[0053] The second interlayer dielectric layer 160 is located on the first interlayer dielectric layer 150.

[0054] The source/drain metal traces 220 extend through the first interlayer dielectric layer 150 and the second interlayer dielectric layer 160.

[0055] The first insulating layer 170 covers the source/drain metal traces 220 and the second interlayer dielectric layer 160.

[0056] The second insulating layer 180 is located on the first insulating layer 170.

[0057] The anode metal **240** penetrates the first insulating layer **170** and the second insulating layer **180**.

[0058] The pixel defining layer **190** is located on the anode metal **240** and has a communication hole connected to the anode metal **240**.

[0059] In the prior art, the gate metal is usually made of molybdenum (Mo), and the interlayer dielectric layer is usually made of a laminate of silicon oxide (SiO<sub>x</sub>) and silicon nitride (SiN<sub>x</sub>). Since there are many differences in material properties between molybdenum and silicon oxide, there is often a large stress at their interface, therefore molybdenum and silicon oxide cannot be tightly bonded. The stress between them even causes the interlayer dielectric layer to fall off, and generates a gap between the gate metal and the interlayer dielectric layer, thereby seriously affecting the characteristics of the thin film transistor, and seriously affecting the yield of the device.

[0060] Therefore, the present invention provides an organic light emitting diode display panel and manufacturing method thereof, which could solve the technical problem of the falling off of the film layer due to the interface stress between the interlayer dielectric layer and the gate metal in the prior art.

[0061] The present invention provides an organic light emitting diode (OLED) display panel, wherein the display panel includes a substrate **110**, a silicon nitride layer **120**, a silicon oxide layer **130**, a polysilicon layer **140**, a gate metal **210**, a gate buffer layer **210a**, a first interlayer dielectric layer **150**, a second interlayer dielectric layer **160**, source/drain metal traces **220**, a first insulating layer **170**, a second insulating layer **180**, an anode metal **240**, a pixel defining layer **190**, and a light emitting structure over the pixel defining layer **190**. The polysilicon layer **140**, the gate metal **210**, the first interlayer dielectric layer **150**, the second interlayer dielectric layer **160**, and the source/drain metal traces **220** constitute a thin film transistor layer.

[0062] The substrate **110** is usually a rigid substrate such as glass, or a flexible substrate such as a polyimide substrate.

[0063] The silicon nitride layer **120** is located on the substrate **110**, and the silicon oxide layer **130** is located on the silicon nitride layer **120**.

[0064] The polysilicon layer **140** is located on the silicon oxide layer **130**, and the polysilicon layer **140** includes heavily doped source and drain regions **230** and a channel region between the source and drain regions **230**.

[0065] The gate metal **210** is located on the polysilicon layer **140**, and the gate metal **210** covers the polysilicon layer **140** above the channel region.

[0066] The gate buffer layer **210a** is located on the gate metal **210**, the material constituting the gate buffer layer **210a** is an oxide of the gate metal layer **210**, and by oxidizing the gate metal layer, a corresponding oxide is formed on the top thereof to constitute a gate buffer layer. Preferably, the material constituting the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide. Preferably, the gate buffer layer has a thickness of 2 to 5 nm.

[0067] The first interlayer dielectric layer **150** is located on the polysilicon layer **140**, and the material thereof is silicon oxide. The first interlayer dielectric layer **150** covers the gate metal **210** and the polysilicon layer **140** that is not covered by the gate metal **210**.

[0068] The second interlayer dielectric layer **160** is located on the first interlayer dielectric layer **150**, and the material thereof is silicon nitride.

[0069] The source/drain metal traces **220** extend through the first interlayer dielectric layer **150** and the second interlayer dielectric layer **160**.

[0070] The first insulating layer **170** covers the source/drain metal traces **220** and the second interlayer dielectric layer **160**.

[0071] The second insulating layer **180** is located on the first insulating layer **170**.

[0072] The anode metal **240** penetrates the first insulating layer **170** and the second insulating layer **180**.

[0073] The pixel defining layer **190** is located on the anode metal **240** and has a communication hole connected to the anode metal **240**.

[0074] In the present invention, after the gate metal (molybdenum) is completed, a thin layer of dense molybdenum oxide of about 2 to 5 nm is formed as a gate buffer layer over the gate dielectric layer by oxidation, and then an interlayer dielectric layer is deposited. Since the surface tension of the molybdenum oxide is between the surface tension of the molybdenum and the surface tension of the interlayer dielectric layer, the molybdenum oxide can effectively reduce the interface stress between the gate metal and the interlayer dielectric layer to prevent the occurrence of falling off after deposition of the interlayer dielectric layer, whereby the characteristics of the thin film transistor can be improved, and the yield of the device can be greatly increased.

[0075] The present invention also provides a method of manufacturing an organic light emitting diode (OLED) display panel, wherein the method includes the steps of:

[0076] providing a substrate;

[0077] forming a polysilicon layer positioned on the substrate, forming heavily doped source/drain regions in the polysilicon layer, the source/drain regions being spaced from each other a distance, and a lightly doped channel region in the polysilicon layer and between the source/drain regions;

[0078] forming a gate dielectric layer positioned on the polysilicon layer;

[0079] forming a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

[0080] forming a gate buffer layer positioned on the gate dielectric layer;

[0081] forming an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

[0082] forming a source/drain region trace layer penetrating through the gate dielectric layer and the interlayer dielectric layer; and

[0083] forming a light emitting structure connected to the source/drain region trace layer.

[0084] The above method will be described in detail below with reference to the accompanying drawings. First, referring to FIG. 2, a substrate **110** is provided, and a silicon nitride layer **120**, a silicon oxide layer **130**, a polysilicon layer **140**, a gate metal **210**, and a gate buffer layer **210a** are sequentially formed on the substrate **110**.

[0085] The substrate **110** is usually a rigid substrate such as glass, or a flexible substrate such as a polyimide substrate.

[0086] The silicon nitride layer 120 is located above the substrate 110, and the silicon oxide layer 130 is located on the silicon nitride layer 120.

[0087] The polysilicon layer 140 is located on the silicon oxide layer 130, and the polysilicon layer 140 includes a heavily doped source and drain regions 230 and a channel region between the source and drain regions 230.

[0088] The gate metal 210 is located on the polysilicon layer 140, and the gate metal 210 covers the polysilicon layer 140 above the channel region.

[0089] The gate buffer layer 210a is located on the gate metal 210, the material constituting the gate buffer layer 210a is an oxide of the gate metal layer 210, and by oxidizing the gate metal layer, a corresponding oxide is formed on the top thereof to constitute a gate buffer layer. Preferably, the material constituting the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide. Preferably, the gate buffer layer has a thickness of 2 to 5 nm.

[0090] Referring to FIG. 3, after the gate buffer layer 210a is deposited, a first interlayer dielectric layer 150, a second interlayer dielectric layer 160, and source/drain metal traces 220 are sequentially formed thereon.

[0091] The first interlayer dielectric layer 150 is located on the polysilicon layer 140, and the material thereof is silicon oxide. The first interlayer dielectric layer 150 covers the gate metal 210 and the polysilicon layer 140 that is not covered by the gate metal 210.

[0092] The second interlayer dielectric layer 160 is located on the first interlayer dielectric layer 150, and the material thereof is silicon nitride.

[0093] The source/drain metal traces 220 extend through the first interlayer dielectric layer 150 and the second interlayer dielectric layer 160.

[0094] After that, see FIG. 4, a first insulating layer 170, a second insulating layer 180, an anode metal 240, a pixel defining layer 190, and a light emitting structure over the pixel defining layer 190 are sequentially formed after the source/drain metal traces 220 are formed.

[0095] The first insulating layer 170 covers the source/drain metal traces 220 and the second interlayer dielectric layer 160.

[0096] The second insulating layer 180 is located on the first insulating layer 170.

[0097] The anode metal 240 penetrates the first insulating layer 170 and the second insulating layer 180.

[0098] The pixel defining layer 190 is located on the anode metal 240 and has a communication hole connected to the anode metal 240.

[0099] In the present invention, the technique of forming the substrate 110, the silicon nitride layer 120, the silicon oxide layer 130, the polysilicon layer 140, the gate metal 210, the gate buffer layer 210a, the first interlayer dielectric layer 150, the second interlayer dielectric layer 160, the source/drain metal trace 220, the first insulating layer 170, the second insulating layer 180, the anode metal 240, the pixel defining layer 190, and the light emitting structure over the pixel defining layer 190 is a mature process in the art and will not be described in detail herein.

[0100] The present invention improves the thin film transistor of the existing organic light emitting diode display panel and the manufacturing method thereof. After the gate metal molybdenum is completed, a thin layer of dense molybdenum oxide of about 2 to 5 nm is formed as a gate

buffer layer over the gate dielectric layer by oxidation, and then an interlayer dielectric layer is deposited. Since the surface tension of the molybdenum oxide is between the surface tension of the molybdenum and the surface tension of the interlayer dielectric layer, the interface stress between the molybdenum and the interlayer dielectric layer can be well lowered to prevent the occurrence of falling off after deposition of the interlayer dielectric layer, whereby the characteristics of the thin film transistor can be improved, and the yield of the device can be greatly increased.

[0101] As is understood by persons skilled in the art, the foregoing preferred embodiments of the present disclosure are illustrative rather than limiting of the present disclosure. It is intended that they cover various modifications and that similar arrangements be included in the spirit and scope of the present disclosure, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. An organic light emitting diode (OLED) display panel, wherein the display panel comprises a substrate, a thin film transistor layer positioned on the substrate, and a light emitting structure positioned on the thin film transistor layer and connected to a source/drain region trace layer in the thin film transistor layer;

wherein the thin film transistor layer comprises:

a polysilicon layer positioned on the substrate, the polysilicon layer has heavily doped source/drain regions spaced from each other a distance and a lightly doped channel region located between the source/drain regions;

a gate dielectric layer positioned on the polysilicon layer; a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

a gate buffer layer positioned on the gate dielectric layer; and

an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

wherein the source/drain region trace layer penetrates through the gate dielectric layer and the interlayer dielectric layer; and

wherein a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

2. The OLED display panel according to claim 1, wherein a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

3. The OLED display panel according to claim 1, wherein the interlayer dielectric layer comprises a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

4. An organic light emitting diode (OLED) display panel, wherein the display panel comprises a substrate, a thin film transistor layer positioned on the substrate, and a light emitting structure positioned on the thin film transistor layer and connected to a source/drain region trace layer in the thin film transistor layer;

wherein the thin film transistor layer comprises:  
 a polysilicon layer positioned on the substrate, the polysilicon layer has heavily doped source/drain regions spaced from each other a distance and a lightly doped channel region located between the source/drain regions;  
 a gate dielectric layer positioned on the polysilicon layer;  
 a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;  
 a gate buffer layer positioned on the gate dielectric layer;  
 and  
 an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;  
 wherein the source/drain region trace layer penetrates through the gate dielectric layer and the interlayer dielectric layer.

**5.** The OLED display panel according to claim 4, wherein a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

**6.** The OLED display panel according to claim 4, wherein a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

**7.** The OLED display panel according to claim 4, wherein the interlayer dielectric layer comprises a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

**8.** The OLED display panel according to claim 5, wherein the gate buffer layer has a thickness of 2 to 5 nm.

**9.** A method of manufacturing an organic light emitting diode (OLED) display panel, wherein the method comprises the steps of:

providing a substrate;  
 forming a polysilicon layer positioned on the substrate,  
 forming heavily doped source/drain regions in the polysilicon layer, the source/drain regions being spaced

from each other a distance, and a lightly doped channel region in the polysilicon layer and between the source/drain regions;

forming a gate dielectric layer positioned on the polysilicon layer;

forming a gate metal layer positioned on the gate dielectric layer, the gate metal layer only covering the gate dielectric layer over the channel region;

forming a gate buffer layer positioned on the gate dielectric layer;

forming an interlayer dielectric layer covering the gate dielectric layer, the gate metal layer, and the gate buffer layer;

forming a source/drain region trace layer penetrating through the gate dielectric layer and the interlayer dielectric layer; and

forming a light emitting structure connected to the source/drain region trace layer.

**10.** The method of manufacturing an OLED display panel according to claim 9, wherein a material constituting the gate buffer layer is an oxide of the gate metal layer, and by oxidizing the gate metal layer, the oxide is formed on a top of the gate metal layer to form the gate buffer layer.

**11.** The method of manufacturing an OLED display panel according to claim 9, wherein a material of the gate metal layer is molybdenum, and the material constituting the gate buffer layer is molybdenum oxide.

**12.** The method of manufacturing an OLED display panel according to claim 9, wherein the interlayer dielectric layer comprises a first dielectric layer and a second dielectric layer, and wherein a material of the first dielectric layer is silicon oxide, the second dielectric layer is positioned on the first dielectric layer, and a material of the second dielectric layer is silicon nitride.

**13.** The method of manufacturing an MED display panel according to claim 9, wherein the gate buffer layer has a thickness of 2 to 5 nm.

\* \* \* \* \*

专利名称(译)	有机发光二极管显示面板及其制造方法		
公开(公告)号	<a href="#">US20200203454A1</a>	公开(公告)日	2020-06-25
申请号	US16/467994	申请日	2018-11-22
[标]发明人	LI SONGSHAN		
发明人	DING, WU LI, SONGSHAN		
IPC分类号	H01L27/32 H01L51/56		
CPC分类号	H01L51/56 H01L27/3258 H01L2227/323 H01L27/3246 H01L27/3262 H01L27/1214		
优先权	201811213431.0 2018-10-18 CN		
外部链接	<a href="#">Espacenet</a>	<a href="#">USPTO</a>	

摘要(译)

提供了一种有机发光二极管显示面板及其制造方法。显示面板包括基板，薄膜晶体管层和发光结构，其中，薄膜晶体管层包括多晶硅层，位于多晶硅层上的栅极介电层，位于栅极介电层上的栅极金属层 栅极绝缘层位于栅极电介质层上，层间电介质层覆盖栅极电介质层，栅极金属层和栅极缓冲层。

